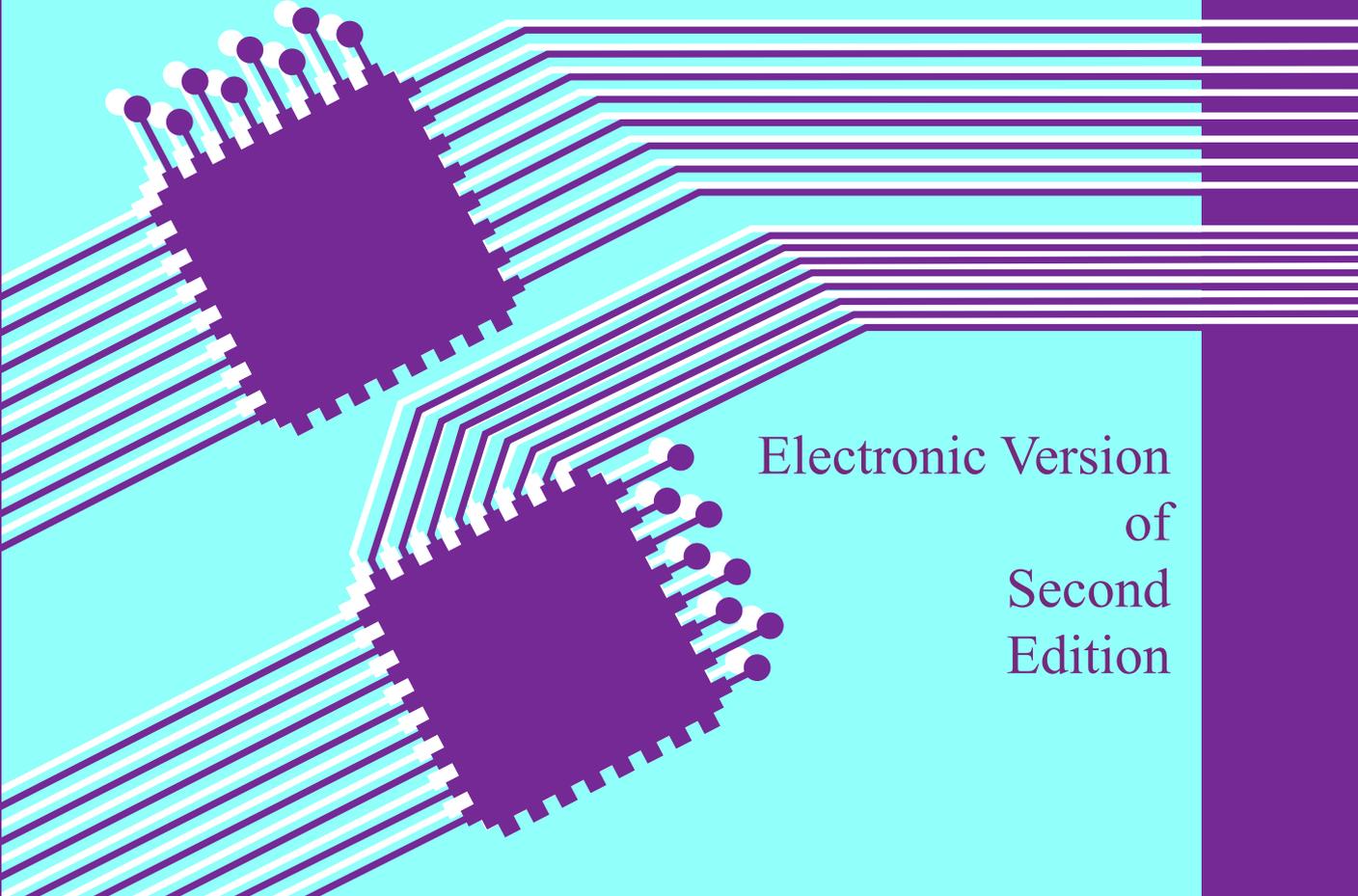


Sample pages from...

The Economics of Automatic Testing

Chapter 4
A primer of test economics

Brendan Davis



Electronic Version
of
Second
Edition

Copyright Notice

“The Economics of Automatic Testing”

Published by
Brendan Davis, Cahir, County Tipperary, Ireland.

Copyright: 1982 (first edition),
1994 (second edition),
2012 (electronic edition) Brendan Davis

Notice of Rights

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written permission of the author and copyright holder.

Copyright of the two printed editions was held by McGraw-Hill International (UK) Ltd. and reverted to the author when the second edition was declared ‘out of print’.

Notice of Liability

The information in this book is distributed on an ‘As Is’ basis without warranty. While every precaution has been taken in the preparation of the book the author and publisher have no liability to any person or entity with respect to loss or damage caused or alleged to be caused either directly or indirectly by the information or instructions contained in this book or by any computer or calculator software and hardware described in it.

Conversion to electronic formats by...

Suirvale Design & Print, Cahir, County Tipperary, Ireland

We do not really need to concern ourselves with conditional events so let us look at a few examples of the others to clarify the differences.

Mutually exclusive events

At a test stage the UUT may pass or it may fail the test. Either of these events will exclude the other so they are mutually exclusive. There are two possible outcomes. Similarly, an analog test to predefined limits has three possible outcomes that are mutually exclusive. The test result may be above the high limit, below the low limit or it may be between the limits (within specification). When mutually exclusive events are involved, a very simple rule exists that says that the probability that anyone of the events will take place is determined by adding up the individual probabilities. This is typically written like this...

$$P(A \text{ or } B \text{ or } C) = P(A) + P(B) + P(C)$$

This is called the *special rule of addition*.

In the two simple examples above, the individual probabilities will add up to 1.0 because at least one of the events considered must occur. A probability of 1.0 denotes absolute certainty. If the probability is 0.7 that a board will pass the test at a specific board test stage, then the probability that it will fail must be 0.3 since one of these mutually exclusive events must occur.

Independent events

Component defects are a good example of independent events because, unlike apples, a bad IC in a batch cannot really affect the others. Most defects on boards can also be considered to be independent of each other but there can be exceptions to this. For instance, the presence of a short on a board that is then powered up on a functional tester may lead to the occurrence of another defect. If the short had been removed before the functional test took place, the second defect would not occur. This is an example of a conditional event. The second defect is conditional on the presence or the absence of the short. However, the added accuracy to be gained by trying to account for this kind of situation is rarely worth the extra effort. The easiest way to account for this effect if you are considering a functional test with no prior shorts test among your strategy options is to modify the expected fault spectrum. For example, if you expect that 40 per cent of defective boards will contain a short, you can make some estimate of what proportion of these would induce additional defects and then add these into your fault spectrum when analysing the cost of the functional test strategy. Naturally these defects would not be included in the fault list for any strategy that would involve the removal of the shorts before any power is applied to the board.

When two events are independent they can occur singly or together. The probability that they will both occur together is determined by multiplying their individual probabilities of occurrence together. This is usually written as...

$$P(A \text{ and } B) = P(A) \times P(B)$$

This is called the *special rule of multiplication* and it holds true regardless of the number of possible events.

For example, if we know that the probability of getting a component-related defect, such as a faulty or a misoriented component, on a board is 0.7 and we also know that the probability of getting a short is 0.55, then we can determine the probability of getting both a component-related defect and a short on the same board by multiplying these probabilities together...

$$P(\text{component}) \times P(\text{short}) = P(\text{both})$$

$$0.70 \times 0.55 = 0.385$$

Therefore, in the long run, over some reasonable quantity of boards we could expect to see 38.5 per cent of the boards containing both a short and a component-related defect. This situation is illustrated graphically in Fig. 4.4.

This information is essential for correctly determining test times, costs and throughput figures for in-circuit testers or any form of tester where it is usual to stop the test if shorts

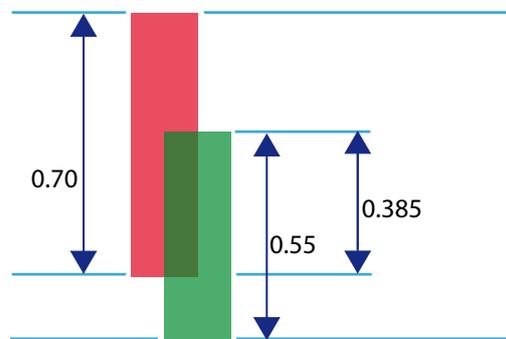


Figure 4.4 Independent events can occur singly or together

are found. The normal practice would be to have the shorts removed at a repair station before returning the boards to the tester to complete the testing. This practice is recommended because the presence of the short can affect the ability of the tester to make other tests on the components. As indicated earlier, when power is applied other damage could occur, but even if no damage is caused the diagnostic performance of the tester will be degraded. For example, the short could be directly across a resistor. This would probably result in the diagnosis of two failures, a short between two nodes and a resistor whose value is below the low limit. Two repair actions would be required, one of them being unnecessary.

The more important fact from an economic analysis point of view is that a board with a short and another type of defect will require one additional visit to the tester and to the repair station-in other words, one more pass around the diagnosis/repair loop. This has obvious implications for both cost and throughput calculations. A board with both kinds of defect will usually pass through the tester three times...

1. Once to find the short (which is then repaired).
2. A second time to find the other defect.
3. And a third time to confirm that the repair action was performed correctly.

Assuming that we know the individual probabilities for a short and for other types of defect (0.55 and 0.7 in the example), we will also need to determine the probability that the board will fail for either reason. This will then also give us the probability that the board will be defect-free. This probability, usually expressed as a percentage, is of course the yield of good boards.

If we simply add the two probabilities we get...

$$0.55 + 0.7 = 1.25$$

This of course is impossible. You cannot have a probability greater than 1.0 because this represents absolute certainty. The problem here is that the *special rule of addition* only applies to mutually exclusive events and not to independent events. A short and some other type of defect can occur independently or both together. They are not mutually exclusive. For independent events we have to use the *general rule of addition*, which is normally written as...

$$P(A \text{ or } B) = P(A) + P(B) - P(A \text{ and } B)$$

For our board test example this formula says that the probability that a board will fail for any reason [P(A or B)] is the probability that there will be a short plus the probability that there will be any other type of defect, minus the probability that both types of defect will occur together. This makes sense because if we do not subtract the probability of both occurring together, these defects will get counted twice.

For our example this becomes...

$$P_{\text{short or other defect}} = 0.55 + 0.7 - (0.55 \times 0.7) = 0.865$$

Now we can determine all of the relevant probabilities. Since the probability of a board failing at all is 0.865 then the probability that it will pass the test (the yield) is...

$$P_{\text{pass}} = 1.0 - 0.865 = 0.135$$

Since 0.865 fail in total and 0.7 fail due to a fault other than a short, then 0.865 - 0.7, or 0.165, must be the probability that the board will fail due to a short with no other type of defect present.

Similarly, since the probability of a short occurring is 0.55 then 0.865 - 0.55, or 0.315, must be the probability that the board will fail due to a defect other than a short with no other shorts present on the board. We now have a complete picture of the various probabilities that will determine the flow of boards around the diagnosis/repair loop. This in turn will enable us to calculate costs and throughputs with the best possible accuracy...

1. 13.5 per cent of boards will pass. This is the yield.
2. 16.5 per cent of boards will contain shorts.
3. 31.5 per cent of boards will contain other defects.
4. 38.5 per cent of boards will contain both shorts and other defects.

This is illustrated graphically in Fig. 4.5. Hopefully your yield will not be as bad as this. The numbers here were chosen to illustrate what is happening in the test process and are not intended to represent a typical yield situation.

The special rule of multiplication revisited

Let us now take another look at the use of the special rule of multiplication. This you may recall is used to determine the probability of a number of independent events occurring together. Let us assume that you are experiencing component defect rates of 1 per cent. This is an unthinkable figure today but it keeps the maths simple. This would imply that the probability that an individual component is good is 0.99...

$$P_{\text{good}} = 0.99$$

Therefore, if you build a printed circuit board containing 100 components then the probability that you will get 100 good components will be 0.99 multiplied by itself 100 times. This is the same as raising 0.99 to the power of 100. If your calculator has a 'Y to the X' key then you can quickly see that the probability is 0.366...

$$P_{100 \text{ good}} = (0.99)^{100}$$

Therefore 36.6 per cent of the boards will be free from component defects even though 100 components with a 1 per cent defect rate would imply that on average each board would contain one defect. On average they will, but in practice the defective components

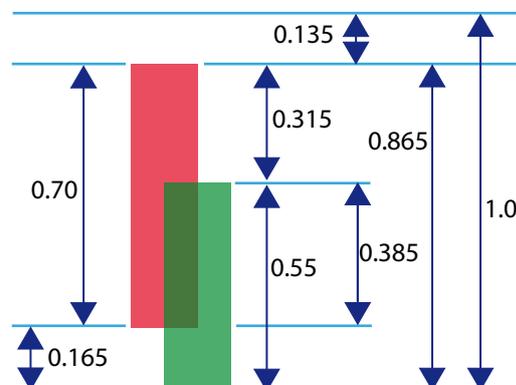


Figure 4.5 Graphical illustration of the example in the text

to simply taking $(1 - \text{FPB})$ as being the yield. Obviously this error reduces at higher yields. With an average of 0.05 FPB the error is only 1.26 per cent.

4.9 Yield

Moving on now from the basic statistical relationships that we need to be aware of, we can take a more detailed look at the issue of yield. As indicated above, yield is the probability that the items being considered are defect-free. More often than not it is expressed as a percentage, and this is simply obtained by multiplying the probability by 100.

The yield you get from a process is a measure of the performance of that process; yield quite simply means money. If you improve the yield of any process it will cost less, the capacity will increase and you will ship better quality products.

We can use some of the techniques outlined in the statistics section to determine the expected yield of a single process step or a complete set of process steps. For example, if we know that the probability that components will be good is 0.995 and that there will be 150 of them on a board, then we know that 0.995 raised to the power of 150 will give us the probability that the board will be free from component defects. This is 0.47. If we also consider that the bare board that these components will be assembled on to has a P_{good} of 0.90 then the yield will now be...

$$0.47 \times 0.90 = 0.42$$

If we also know that the probability that we will assemble the board correctly is 0.90 and that we will solder it without defects is 0.95, then our overall yield going into the first test stage will be...

$$0.42 \times 0.90 \times 0.95 = 0.36$$

Therefore each step in the manufacturing process has an error rate associated with it. The defects introduced at each stage are cumulative and we can estimate the overall yield of a process by using the special rule of multiplication. This example is shown graphically in Fig. 4.6. This shows what I call a '*yield progression*'. As the product progresses through the process, the yield will change. For a manufacturing process step the yield will become smaller. Following a test step, with repair, the yield will increase. The yield will also decrease following any stressing step such as a burn-in or a vibration screen. For any

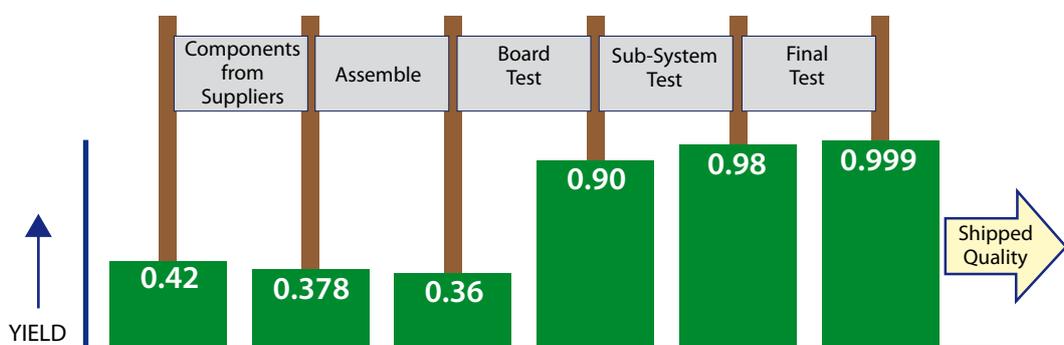


Figure 4.6 The 'Yield Progression'

test stage where repair is not possible, as with semiconductor component manufacturing, the yield will also increase because defective items will be discarded. However, there will be fewer products as a result of this scrapping of defectives. Component manufacturers often refer to this as 'shrinking' because this is lost product that cannot be recovered. It is easy to see why yield has always been such a critical issue in the semiconductor industry. With so many process steps involved, a small improvement at each will make a big difference to the capacity and the profitability of a production line.

Equipment manufacturers are in a somewhat better position because their products are repairable. This may be the reason why they are less paranoid about yield, but, as will become clear from some examples, they ought to be just as concerned about yield as their semiconductor counterparts are. Since they can repair or re-work their products, equipment manufacturers can in theory ship 100 per cent of the products that they set out to make. In the yield progression any test or inspection stage should result in an increase in yield as defects are detected and repaired, with no loss of production volumes. The in-circuit test stage will detect the manufacturing defects and some of the component defects. Sub-system test will find additional defects, as will the final system test stage. In practice, of course, none of these will detect 100 per cent of all the defects present and some will always slip through to be shipped to the customer.

Therefore the effectiveness of each tester, and that of the overall test strategy, will have a major impact on the yield progression, the cost of achieving any improvement and the number of defects shipped to the field. This then brings us to the subject of fault coverage.

4.10 Fault coverage

Fault coverage is a measure of the ability of a tester to detect defects. Fault coverage can be one of the major differences between competing test systems and will be central to any economic justification for a high-performance tester versus a lower priced model with less performance. Fault coverage affects yield in two ways:

1. It influences the yield 'seen' by the tester.
2. It determines the yield coming out of the tester.

To understand what I mean by this it is necessary to consider that any process stage has an input yield and an output yield. For a manufacturing stage the output yield will be lower than the input yield since the stage will have the possibility of inducing defects. For a test stage the output yield should normally be higher than the input yield since any detected defects will be either repaired or discarded. However, the output yield from a test stage will not be 100 per cent because of the fault coverage limitations. In terms of faults, there will be some faults present on the UUTs entering the test stage that will determine the input yield. There will also be the faults detected by the test stage, which will then be repaired. The difference between these will be the faults that escape detection, and these will determine the output yield from the test stage.

4.11 Apparent yield

The yield that is 'seen' by the test stage is a function of the number of faults that are detected by it rather than the number of faults that are actually present. As the fault coverage drops the yield seen by the test stage will increase. This should be quite obvious because if the fault coverage is so bad that no defects are detected, the yield will appear to be 100 per

cent. For this reason I refer to the yield seen by the tester as the *apparent yield*. Figure 4.7 shows the three yields associated with a test stage. You may recall that the relationship between the number of faults and yield can be expressed by the formula...

$$Y = e^{-FPB}$$

This formula relates the actual yield to the actual number of faults present and so this is the formula for the input yield to the stage. The apparent yield (Y_a) at the tester is a function of the number of detected faults per board (DFPB) and so can be expressed as...

$$Y_a = e^{-DFPB}$$

Alternatively, since the number of detected faults is a function of the number of actual faults and the fault coverage of the test stage, we can also express Y_a as follows...

$$Y_a = e^{-(FPB)FC}$$

where FC is the fault coverage expressed as a factor, as opposed to the usual way of expressing it as a percentage. The output yield (Y_o) from the stage is a function of the number of escaping faults (EFPB) and can be expressed as...

$$Y_o = e^{-EFPB}$$

Output yield can also be expressed as...

$$Y_o = e^{-(FPB-DFPB)} \quad \text{or} \quad Y_o = e^{-[FPB-FPB(FC)]}$$

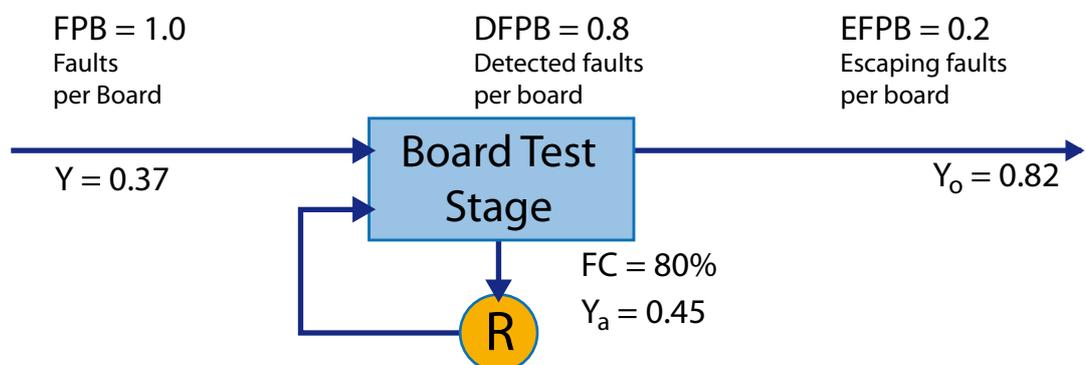


Figure 4.7 Input yield, apparent yield and output yield

As an example, if we have 1 FPB coming into this test stage and the fault coverage is 80 per cent, then we will have 0.8 DFPB and 0.2 EFPB. This will give us an input yield of 0.37 or 37 per cent, an apparent yield at the tester of 0.45 or 45 per cent and an output yield from this stage of 0.82 or 82 per cent. The difference between the input yield and the apparent yield is one reason why some companies think that their manufacturing yields are higher than they really are. There are, however, other factors that may influence this view which relate to the way in which data is collected from the production process.

At any point in time there will be batches of newly manufactured boards and batches of repaired boards entering a test stage. If the data collection system being used differentiates between these batches then the yield measured at the tester for the new boards should be close to the apparent yield that could be calculated from a knowledge of the FPB and the fault coverage of the test stage. If the data collection system does not differentiate between these batches of new and repaired boards, then the yield measured from the data would be very much higher than any calculated value because the high yield of the batches of repaired boards will skew the results.

Using the example of 1 FPB and a fault coverage of 80 per cent we determined that the apparent yield would be 45 per cent. Therefore 55 per cent of the boards will fail (be detected) and go off to be repaired. Assuming, for simplicity, that the repair action is performed correctly and that none of the boards with 2 or more defects require a second pass around the diagnosis/repair loop, then the repaired boards will all pass the test when they are re-tested. If the data collection system differentiates between these two batches of boards entering the test stage, then we will see apparent yields of 45 per cent for the newly manufactured boards and 100 per cent for the repaired boards.

4.12 Perceived yield

If the data collection system does not differentiate between these batches then for every 100 boards produced the test stage will see 155 tests, of which 55 fail and 100 pass. The yield based on these numbers will be 100/155 or 0.65 (65 per cent). This is shown in Figure

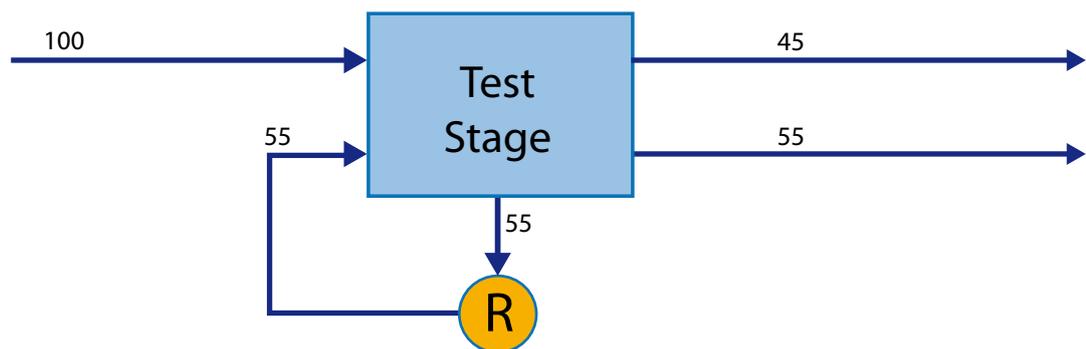


Figure 4.8 The flow of boards around a test and repair cell

4.8. To avoid confusion with apparent yield, which simply accounts for the effect of fault coverage, we call this the *perceived yield* (Y_p). In this example, as in practice, this erroneous measure of yield caused by deficiencies in the method of data collection is usually well above the actual yield of 37 per cent and the true apparent yield of 45 per cent.